Hopping transport in silicon layers with a low content of impurity atoms

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Peaks of the negative differential resistance and a large spread in the transverse hopping conductivity have been observed in thin epitaxial silicon layers with a small area. Anomalously high conductivity has been observed in layers with a low impurity atom density: $N=1\cdot 10^{13}-6\cdot 10^{14}\ \mathrm{cm}^{-3}$. The results of the investigation of the low-temperature conductivity of the samples are explained by transport along extended chains of localized states with electron trapping in two types of traps. A geometry is proposed for the traps that explains well the number and position of the peaks of the negative differential resistance. © *1996 American Institute of Physics.* [S1063-7761(96)01512-0]

1. INTRODUCTION

Hopping conduction along localized states in semiconductors drops exponentially with decreasing density N of the impurity atoms.[1] For example, in silicon this conductivity is impossible to measure experimentally because of its low value, even with $N<1\cdot 10^{16}\ \mathrm{cm}^{-3}$ for atoms with "shallow" energy levels, such as boron, phosphorus, and others.

While investigating transverse hopping transport through thin epitaxial silicon layers, we discovered that layers with a low density of impurity atoms ($N=1\cdot 10^{13}-6\cdot 10^{14}\ \mathrm{cm}^{-3}$) and a definite thickness possess anomalously high conductivity.[2] The present work is devoted to investigation of this conductivity, which cannot be explained by the standard three-dimensional hopping transport. The results obtained are explained by the presence of extended chains of localized states in the layers. These chains connect the opposite surfaces of the layer and the contact regions present on the surfaces. The chains contain two types of traps which trap and confine electrons for some time. A possible mechanism of the formation of such chains in epitaxial silicon layers is also discussed.

2. EXPERIMENTAL PROCEDURE

Silicon layers with hole-type conductivity were grown by molecular-beam epitaxy on strongly doped substrates, which played the role of one of the contacts (the bottom one). The top contacts to the layers had different areas in the SiO_2 windows: from $S=50\times 50$ up to $S=500\times 500\ \mu\mathrm{m}^2$. All contact regions were prepared by means of photolithography and low-temperature technology, including implantation of low-energy boron ions and aluminum metallization. This technology made it possible to obtain ohmic contacts to the layers and prevent diffusion of boron atoms from the substrate and contact regions into the layer. Figure 1 displays a cross section of the prepared structures. Here the current does not spread from the top contact 3 along the surface (this was checked experimentally) because of the presence of a potential barrier for charge carriers at the boundary with the insulator. It is known that such a barrier exists at the boundary between SiO_2 and n-type silicon. Therefore the size of the region of flow of the transverse current in the experimental structures is limited in practice to the thickness of the layer and the area of the top contact to the layer.

The layers were grown by molecular-beam epitaxy of silicon with a low background impurity content. This technique was developed at the Institute of Semiconductor Physics of the Siberian Branch of the Russian Academy of Sciences. The impurity density in the structures obtained decreased by five orders of magnitude at the substrate–layer boundary in a layer of thickness 0.1 μm. Such a large density gradient was achieved as a result of the low temperature at which the layers were grown ($T\sim 800\ ^\circ\mathrm{C}$) as well as by a special technique for cleaning the surface prior to the epitaxy process. Therefore, under the conditions of molecular-beam epitaxy, the diffusion of impurity atoms from the strongly doped substrate is limited, which makes it possible to obtain silicon layers with a low density of uniformly distributed background impurity $N\sim 1\cdot 10^{13}\ \mathrm{cm}^{-3}$ and no volume hopping conductivity. Layers prepared by this technique were first reported in Ref. 3.

In the present work the epitaxial layers were grown on substrates of single-crystalline silicon with (111) crystallographic orientation (Si (111)) and boron impurity density $N\sim 1\cdot 10^{17}\ \mathrm{cm}^{-3}$. The layers ranged in thickness from 1 to 4.5 μm and the acceptor impurity density ranged from $N\sim 1\cdot 10^{13}\ \mathrm{cm}^{-3}$ up to $N\sim 6\cdot 10^{14}\ \mathrm{cm}^{-3}$. The layer with thickness $d=4.5\ \mu$m had the highest impurity density ($N\sim 6\cdot 10^{14}\ \mathrm{cm}^{-3}$). The structure perfection of the single-crystalline layers was monitored during growth under ultrahigh vacuum conditions by means of electron diffraction. The 7×7 superstructure observed in the diffraction pattern attested to the atomic purity of the surface. Control measurements of the impurity atom density profiles in the layers were performed by the $C-V$ method at a temperature of $T=300$ K. A mercury probe of diameter 200 μm was used as contact. The impurity profiles were found to be quite sharp: The width of the transitional region with a variable density was less than 0.1 μm. The uniformity of the impurity distribution measured with the aid of the mercury probe was better than 20% over the entire thickness of the layer and over the surface.

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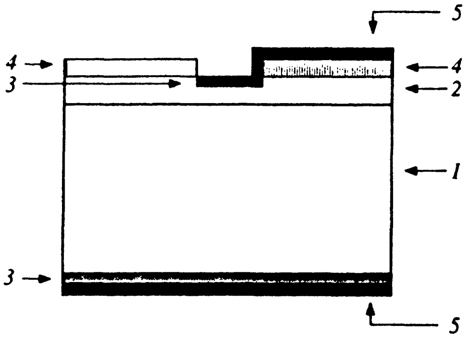

FIG. 1. Cross section of the experimental structures. 1—Strongly doped silicon substrate, 2—epitaxial layer, 3—contact regions, 4—dielectric layer, 5—metal.

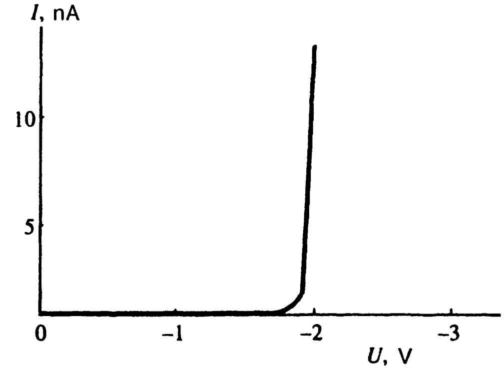

FIG. 2. Current-voltage characteristic of sample No. 1 with layer thickness $d=4.5$ μm; $T=10.0$ K, $S=50\times 50$ μm^2.

The electrical conductivity of the samples was investigated in the temperature range $T=6-60$ K and voltage range -2 V $<U<2$ V. At first glance, the voltage applied to the sample should drop practically to zero in a weakly doped silicon layer, since the boron impurity density in the substrate is quite high. In this case charge carrier transport will be determined by the properties of the layer and not the substrate. This is what actually happens, but the space-charge region in the substrate with one of the two voltage polarities is determined not by the main impurity (boron) but rather by the compensating impurity, whose density is much lower. The width of the space-charge region for the experimental structures in the case when the layer blocks hopping conducting is determined by the expression

$$w=\sqrt{2\varepsilon\varepsilon_0 U/eN_c+d^2}-d, \tag{1}$$

where N_c is the compensating impurity density, e is the electron charge, d is the thickness of the silicon layer, U is the voltage applied to the structure, and ε is the permittivity of the medium. We shall estimate the value of N_c in the substrate on the basis of the temperature dependence of the conductivity measured at the voltage $U=0.5$ V for a sample with no epitaxial layer. The transition from hopping conduction with $\varepsilon_3=5.6$ meV to a section with a weak temperature dependence of the conductivity is observed at $T^*=17$ K. We obtain N_c from the expression

$$N_c=N\exp(-\varepsilon_3/kT^*)=2.2\cdot 10^{15}\ \mathrm{cm}^{-3}.$$

The equation (1) gives the width of the space-charge region for epitaxial layer thickness $d=4.5$ μm and voltage $U=2$ V: $w=0.13$ μm. Therefore the condition $w\ll d$ is satisfied, and charge carrier transport is determined by the properties of the layer.

3. RESULTS

For a number of samples with an epitaxial layer of thickness $d=4.5$ μm, impurity density $N\sim 6\cdot 10^{14}$ cm^{-3}, and contact area $S=50\times 50$ μm^2, no conductivity was observed at temperature $T=10$ K and voltages $0<U<1.5$ V (Fig. 2) (the minimum current measurable with the aid of the experimental apparatus was $I=1\cdot 10^{-14}$ A). The rapid growth of the current in the current–voltage curve at voltage $U=2$ V is apparently due to the "impurity breakdown" phenomenon. The absence of conduction is consistent with the well-known ideas of hopping transport. For such a low density of impurity atoms in silicon the hopping conductivity should indeed be negligibly small. At the same time, a high conductivity was observed for other samples from this series under the same measurement conditions, and a large variation in the conductivity (approximately by a factor of 10^4) over the samples is observed. As the area of the top contact to the layer increases, the variation in the conductivity vanishes. A high transverse conductivity is observed in samples with thinner (1 μm $<d<4.5$ μm) silicon layers, impurity density in the layers from $N\sim 1\cdot 10^{13}$ cm^{-3} up to $N\sim 1\cdot 10^{14}$ cm^{-3}, and different areas of the top contacts. This conductivity remains practically constant for the samples with the same layer and the same contact area.

For all samples, two sections with activation energies ε_1 and ε_3, corresponding to excitation of electrons from the valence into the impurity band and hopping transport, are observed in plots of the logarithm of the conductivity versus the inverse temperature:

$$\sigma(T)=\sigma_1\exp(-\varepsilon_1/kT)+\sigma_3\exp(-\varepsilon_3/kT). \tag{2}$$

The current–voltage characteristics (IVCs) of the samples at low voltages in the region of hopping conductivity are close to ohmic. For all samples, increasing the temperature to $T\sim 26$ K and the introducing of a conduction band do not change the qualitative form of the IVCs. This shows that there are no substantial potential barriers near the boundary of the epitaxial layer with the substrate and in the contact region.

We return now to samples with epitaxial layer thickness $d=4.5$ μm and top contact area $S=50\times 50$ μm^2. For samples with high conductivity at low voltages ($U=0.5$ V) $\sigma(T)$ is described by the law (2) with activation energies $\varepsilon_1=30.6$ meV and $\varepsilon_3=2.3$ meV (Fig. 3). The hopping conductivity is appreciable at temperatures $T<20$ K. A weak temperature dependence of the conductivity is observed at $T=17-20$ K. At higher temperatures conduction with activation energy ε_1 appears. Sections with a negative differential resistance were observed on the IVCs for several samples from this series; these sections appear when the voltage applied to the sample is varied slowly. The number and position of the negative differential resistance peaks is different

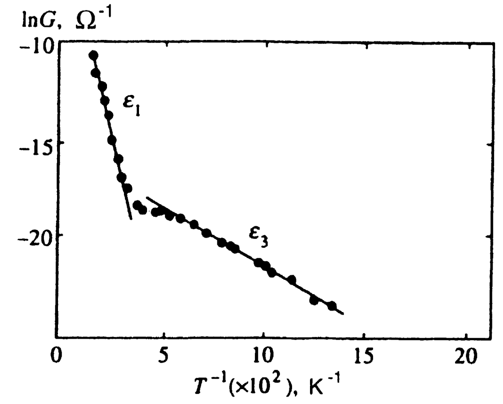

FIG. 3. Temperature dependence of the conductivity for sample No. 2 with epitaxial layer thickness $d = 4.5$ μm, $S = 50 \times 50$ μm^2.

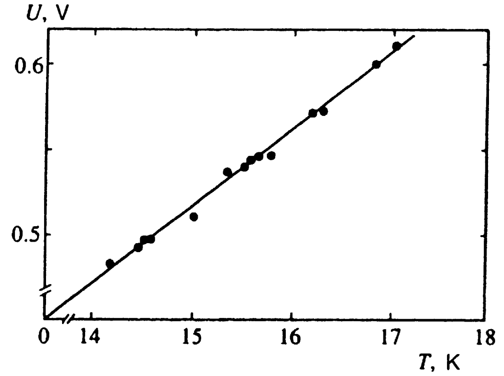

FIG. 5. Temperature dependence of the position of a negative differential resistance peak for sample No. 2. $d = 4.5$ μm, $S = 50 \times 50$ μm^2.

for different samples. Peaks of negative differential resistance on the IVCs of two samples are clearly seen in Fig. 4. The peaks are reliably recorded at $T = 13-20$ K, which corresponds to the region where the temperature-dependence of the conductivity is weak. At higher temperatures the position of the peaks in the IVCs becomes unstable in time. The temperature dependence of the position of a negative differential resistance peak for one sample is presented in Fig. 5. The experimental points lie near the straight line passing through the coordinate origin T, $U = \{0, 0\}$. The same linear relation was obtained in Refs. 4 and 5 for the flat section, observed there, with a negative differential resistance in the IVCs of silicon samples. The appearance of negative differential resistance in the samples was attributed to the capture of electrons in numerous traps, consisting of dead-end branches of a cluster formed from states localized on impurity atoms. The conductivity decreases according to the law

$$\sigma(E) \propto \sigma(0) \exp(-eEL/2kT), \tag{3}$$

where e is the electron charge, E is the intensity of the electric field, and L is the size of a trap. The smaller the trap and the higher the temperature, the easier it is for a trapped electron to escape. The position of a negative differential resistance peak on the voltage scale is found from the relation $E = 2kT/eL$. Using this expression, we obtain for sample No. 2 (see Fig. 4) $L \sim 13$ nm. The presence of not one but several peaks for other samples could be associated with the large number of traps, and as a result of their different size, there should be a spread in the position of the peaks on the voltage scale.

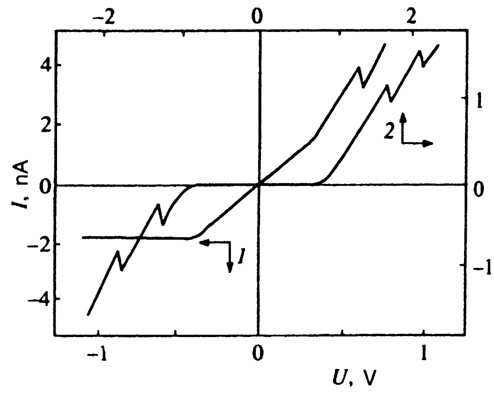

FIG. 4. Current-voltage characteristics of samples with a layer of thickness $d = 4.5$ μm, $S = 50 \times 50$ μm^2. *1*—Sample No. 2, $T = 15.0$ K, *2*—sample No. 3, $T = 11.6$ K.

From the expression $\varepsilon_3 = 0.99 e^2 N^{1/3}/\varepsilon$ (Ref. 3) we obtain $N = 7.3 \cdot 10^{15}$ cm^{-3} for activation energy $\varepsilon_3 = 2.3$ meV (Fig. 3) and the average distance between the localization centers $r = (4\pi N/3)^{-1/3} = 32$ nm.

4. CONCLUSIONS

The following conjectures can be made on the basis of the results obtained.

In the experimental silicon layers in the temperature range corresponding to hopping conduction transport occurs along extended chains of localized states. The large spread in the conductivity over the samples with top contact area $S = 50 \times 50$ μm^2 and a layer of thickness $d = 4.5$ μm attests to the small number of chains. Some samples from this series, in which conductivity was not observed, do not contain even one extended chain connecting the contacts. An estimate of the chain density in a layer gives $10^4 - 10^5$ cm^{-2}. Two kinks, which could be associated with switching of conduction between chains, are clearly seen in the IVC of sample No. 2 (curve 1 in Fig. 4) in the regions of positive and negative voltages. The presence of traps in the form of broken links or S-shaped sections in some chains, for certain ratios of the electric field intensity and temperature, results in trapping of electrons and a decrease of the current, and peaks with a negative differential resistance appear on the IVCs. The peaks are sharp, which could attest to transport along a limited number of chains. For a three-dimensional cluster of localized states, trapping of electrons in one part of the cluster results in current redistribution over the remaining branches and therefore sharp changes in the conductivity of the sample do not occur. In this case only one, quite flat, section with negative differential resistance appears in the IVC,[4,5] while in one of our samples four peaks were observed simultaneously, and the peaks were so sharp that we were not able to determine the differential resistance. The position of the negative differential resistance peaks in the

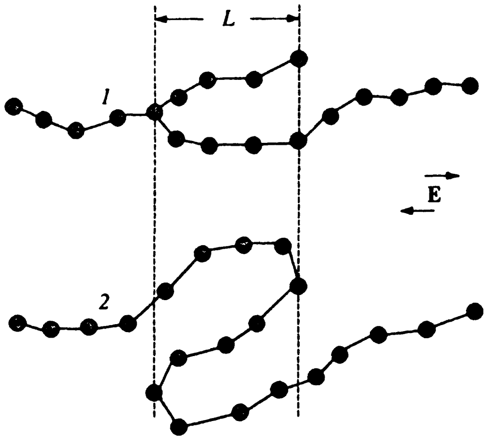

FIG. 6. Geometry of the traps: 1—In sample No. 2; 2—in sample No. 3 (IVCs 1 and 2, respectively, in Fig. 4).

IVC relative to the origin as well as their number open the way for a conjecture about the geometry of the traps, which are depicted in Fig. 6. For sample No. 2 (IVC 1 in Fig. 4) a trap has the form of a broken link in a chain of localized states that is capable of trapping electrons only for one polarity of the external electric field. For sample No. 3 (IVC 2 in Fig. 4) there are two S-shaped traps, which trap charge carriers with both directions of the electric field. Therefore the symmetry in the position of the four negative differential resistance peaks relative to the origin of the coordinates for sample No. 3 and the presence of only one peak for sample No. 2 can be explained.

A large spread in the transverse hopping conductivity was observed only in samples with the thickest epitaxial layer and the smallest contact area. As the thickness of the layer containing chains of different length decreases and the contact area to this layer increases, an increasingly large number of chains participates in electron transport, and for this reason the conductivity here remains virtually constant in magnitude for samples with the same contact area.

Chains of localized states in the experimental epitaxial silicon layers can be formed by impurity atoms trapped by extended structural defects. The positions of the atoms along a defect apparently should be uncorrelated. The absence of a correlation results in localization of electronic states on impurity atoms and the appearance of an activational conductivity with energy ε_3. The density of intrinsic structural defects, which we observed in the experimental samples with the aid of electron microscopy, was equal to $\sim 10^4$ cm^{-2}, which is comparable to the "chain density" obtained from conductivity measurements.

The possible mechanisms for the trapping of impurity atoms by extended structural defects are quite difficult to analyze. Simple estimates show that on account of the short diffusion length, diffusion of impurity atoms in the silicon layer during growth of the layer and during preparation of the contacts cannot explain the formation of the chains we studied, with density 10^4-10^5 cm^{-2}. Apparently, during growth this process can proceed as a result of the diffusion of impurity atoms along the surface and trapping by extended defects, which emerge at the surface.

Numerous investigations of point defects, whose structure has been studied in greatest detail, mainly by the ESR method, show that impurity atoms can occupy both site and different interstitial positions near a defect in the crystal lattice of silicon. Choosing for definiteness an aluminum atom in silicon, we can turn to Refs. 6 and 7 where aluminum was observed in different interstitial positions. Since point defects are the main structural material for many extended defects, this result indicates a real possibility of an uncorrelated arrangement of impurity atoms along extended defects in silicon. In this case, it is easy to imagine a meandering chain, extended along a linear defect, for example, a dislocation, in which the impurity atoms are located at different distances from the defect and occupy different positions in the lattice. In such a chain traps for electrons can form: S-shaped sections and branches consisting of several impurity atoms. Types of structural defects which, by trapping impurity atoms, could form extended chains of localized states were not considered in the present paper. It is also impossible to rule out the possibility that since the impurity atoms are structural defects in the crystal lattice of the silicon and are capable of interacting with one another, during growth of a layer impurities are incorporated into a chain without the participation of extended defects. Localized states, which are responsible for the hopping conduction in the layers studied, close to the valence band are characteristic for "shallow" impurity states, and for this reason it is unlikely that the chains studied here are formed only by extended structural defects without the participation of impurity atoms.

Neither I nor other investigators known to me observed anomalously high hopping conductivity in Si(100) layers with a low content of impurity atoms. It is well known that such epitaxial layers have a lower density of structural defects than Si(111) layers. Apparently, the area per chain of localized states in our experimental Si(111) layers and the characteristic length of such a chain were close to the contact area and layer thickness, respectively, and this created favorable conditions for observing these chains.

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